JACOB MONDORA

linkedin.com/in/jacob-mondora-b56289251 | jacobmondora2026@u.northwestern.edu | 330-554-0755

EDUCATION

Northwestern University *Expected Jun 2026*

- B.S. **Computer Engineering**, *Minor in* **Machine Learning and Data Science**
- **Relevant Coursework:** Computer Architecture, ASIC and FPGA Design, Design Automation in VLSI, Computer Architecture Projects, Real-Time Digital Systems Design & Verification with FPGAs, Electronics, Data Structures & Algorithms
- **Involvement & Leadership:** IEEE Technical Program, McCormick Student Advisory Board, Robotics Club

WORK EXPERIENCE

Huntington Securities, Inc., *Trading Systems & Analytics Intern* *Summer 2025*

- Deployed an automated ETL pipeline (Python, SQL, AWS) that parsed and validated 700+ vendor data files, standardizing position and account datasets for downstream analytics, and reduced processing time by over 95%.
- Architected daily capital & P/L dashboard consolidating broker-dealer market values, capital usage, and pipeline impact, eliminating the need for multi-source manual reporting.
- Engineered Bloomberg EAP ingestion: developed OAuth2-authenticated pipeline for catalog request submission and SSE event listening, automating retrieval of market data for quantitative capital analysis.

Quantinuum, *Data Visualization Engineering Intern* *Summer 2024*

- Analyzed 12+ key quantum system metrics using Python and statistical modeling to identify factors affecting quantum computing performance, enabling physicists and engineers to make data-driven optimization decisions.
- Developed a dataset of 10,000+ synthetic and lab-generated laser beam images to cover alignment edge cases for training computer vision models.
- Deployed a CNN-based image processing tool (Python, PyTorch/TensorFlow) used to enable the automatic calibration of quantum hardware in a closed-loop system.

Carmel Software, *Project Researcher* *Summer 2023*

- Utilized Building Information Modeling (BIM) software, such as Revit, to develop detailed structural models for fire-safety analysis.
- Applied fire-safety software, including FDS, Pyrosim, and Pathfinder, to execute simulations and conduct analyses to enhance fire-safety measures.

PROJECTS & OTHER EXPERIENCE

5-Stage Pipelined RISC-V CPU (Verilog)

- Designed a 32-bit RISC-V (RV32IM) processor in Verilog, including a single-cycle architecture and a fully pipelined 5-stage implementation (IF/ID/EX/MEM/WB).
- Implemented complete hazard handling, including data forwarding, load-use stalls, branch flushing, and multi-cycle control for long-latency instructions.
- Built custom test programs and verification infrastructure to validate correctness across the RV32IM instruction set.

FPGA-Powered Tank Duel Game (VHDL)

- Designed a real-time hardware game system using 20+ VHDL modules, integrating PS/2 keyboard control, VGA graphics, LCD output, and score logic on an Intel DE2-115 FPGA.
- Developed custom hardware game logic, including tank movement controllers, multi-speed keyboard-driven input decoding, bullet firing FSMs, and a combinational collision-detection module synchronized to the VGA pixel clock.
- Implemented a 100 MHz PLL-driven clocking architecture and optimized RTL to meet timing across all subsystems.

AI Chatbot for Course Evaluations

- Built AI chatbot for querying Northwestern course evaluations (CTECs), enabling real-time responses from natural language queries.
- Designed an embedding pipeline for 10,000+ student essay evaluations across 450+ different NU courses, storing vectors in AWS RDS.
- Automated parsing and integration of course metadata into a database with user-specific features like chat history.

SKILLS

Hardware Design: Digital Logic, FPGA and ASIC Design, Circuits, Verilog, VHDL, VLSI Design, OpenROAD

Software: Python, Java, C++, SQL, MATLAB, AWS, Machine Learning, Building Information Modeling (BIM)